



Detector Support Group

We choose to do these things "not because they are easy, but because they are hard".

Weekly Report, 2021-08-04

Summary

Hall A – HV

Brian Eng

- Developing Python script to generate EPICS *Main Menu* Phoebus screen (Hall A will be using Phoebus instead of CSS-BOY)

Hall A – SoLID

Mary Ann Antonioli, Pablo Campero, Brian Eng, Mindy Leffel, Marc McMullen

- Determined the type and number of 2nd level terminal strips required to connect strain gauge and load cell sensors (32 and 8, respectively)
- Updated *Cable List* spreadsheet

Hall B – RICH-II

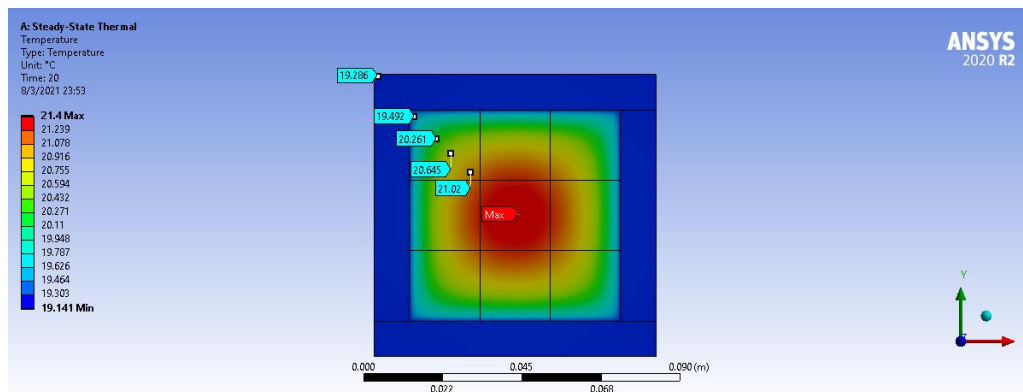
Mary Ann Antonioli, Peter Bonneau, Pablo Campero, Brian Eng, George Jacobs, Tyler Lemon, Marc McMullen

- Developing Hardware Interlock LabVIEW User Interface
- Researched TE Connectivity's latching USB connectors for hardware interlock chassis
- Developing air cooling P&I diagram and components list
- Revising backplane PCB design
 - ★ Added surface-mount LEDs to indicate power status for each sensor

Hall C – NPS

Mary Ann Antonioli, Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, George Jacobs, Mindy Leffel, Tyler Lemon, Marc McMullen

- Developing Hardware Interlock System program LabVIEW front panel; added average of standard deviations for each crystal zone (front and back) to the *Plots* tab
- Using ANSYS, conducted a thermal analysis of a 3x3 block of PbWO₄ crystal surrounded by 1 cm thick copper on four sides



Screenshot of 3x3 block of PbWO₄ crystals inside of a 1 cm thick Cu shell; maximum temperature of the central crystal is 21.4°C



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- Generated MySQL database for HV supply cable testing analysis plots
- Completed final steps for nine HV supply cables: 39 of 40 complete – cut screws, heated heat shrink, replaced jumper wires, and repaired 55 wires
- Labeled 19 cables: 39 of 40 complete
- Started cutting cables to three foot lengths for the CAEN HV test stand

EIC

Brian Eng

- Developing detailed schedule; initial drafts done for all tracking detectors